**Chapter-6 (Practice Questions Lecture-23)**

1. Show the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:

(a) 1010111100 (b) 1111000011 (c) 1011110011 (d) 1000000001

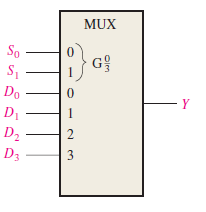
1. Show the logic required to convert a 10-bit Gray code to binary and use that logic to convert the following Gray code words to binary:

(a) 1010111100 (b) 1111000011 (c) 1011110011 (d) 1000000001

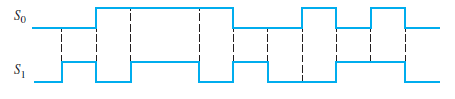
1. For the multiplexer in Figure1, determine the output for the following input

states: D0 = 1, D1 = 0, D2 = 0, D3 = 1,

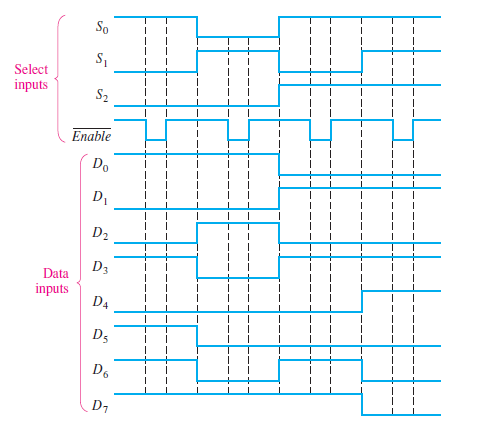
1. S0 = 0, S1 = 1 (b) S0 = 1, S1 = 1 (c) S0 = 1, S1 = 0

Figure1

1. If the data-select inputs to the multiplexer in above Figure1 are sequenced as shown by the waveforms in Figure2, determine the output waveform with the data inputs specified in Problem3.

Figure2

1. The waveforms in Figure3 are observed on the inputs of a 74HC151 8-input multiplexer. Sketch the Y output waveform.



1. Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is a serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is first in the sequence, with its LSB first, and it should appear in the first 4-bit positions of the output.
2. Implement the following Boolean function using decoder.

F (A, B, C,D) = Σ ( 1, 2, 3, 7,9,13,15)

1. Implement the logic function in table by using a 74S151 8 input data selector/multiplexer. X(A3, A2, A1, A0) = ∑(2,3,4,8,9,10,11,15)
2. Implement a full adder circuit by using:

(a)3 – to - 8 line Decoder (b) 4 X 1 Multiplexers.

1. Construct a 16 X 1 multiplexer with two 8x1 and one 1x4 multiplexers. Use block diagrams.